Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled) A memory module buffer comprising:

a host-side memory channel port and a memory device channel port;

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type; and

a memory device access controller to respond to a command having an implicit command type by generating at least one explicit memory access command to the memory device channel port.

2. (Cancelled) The memory module buffer of claim 1, wherein the at least one implicit command type includes at least one implicit write command with a command format that specifies a first region of memory to be written to and includes less explicit write data than would be needed to fill the region of memory, the buffer further comprising a write data generator to form implicit write data in accordance with the implicit write command.

3. (Currently Amended) ~~The memory module buffer of claim 2,~~ A memory module buffer comprising:

a host-side memory channel port and a memory device channel port;

a command decoder to decode commands received at the host-side memory channel

port, the commands including at least one implicit command type, wherein the at least one implicit command type includes at least one implicit write command with a command format that specifies a first region of memory to be written to and includes less explicit write data than would be needed to fill the region of memory, the buffer further comprising a write data generator to form implicit write data in accordance with the implicit write command and further wherein the at least one implicit write command includes a copy command specifying a second region of memory to be read from to form the implicit write data, the memory device access controller responding to the copy command by causing the buffer to read data from the second region of memory to form the implicit write data; and

a memory device access controller to respond to a command having an implicit command type by generating at least one explicit memory access command to the memory device channel port.

4. (Original) The memory module buffer of claim 3, wherein when the second region of memory is smaller in size than the first region of memory, the write data generator forms implicit write data by repeating at least some data from the second region of memory.

5. (Currently Amended) The memory module buffer of claim ~~2~~ 3, wherein the at least one implicit write command includes a command comprising a data value, and wherein the write data generator forms implicit write data by repeating the data value for multiple addresses throughout the first region of memory.

6. (Currently Amended) The memory module buffer of claim ~~2~~ 3, wherein the at least one implicit write command includes a command indicating that a predefined pattern is to be written to the first region of memory, and wherein the write data generator forms implicit write data by repetitively generating the predefined pattern.

7. (Original) The memory module buffer of claim 6, further comprising a pattern register coupled to the write data generator to store the predefined pattern.

8. (Original) The memory module buffer of claim 6, wherein the predefined pattern is at least partially dependent on the address being written to, and wherein the write data generator forms implicit write data using at least a portion of the address being written to.

9. (Currently Amended) The memory module buffer of claim ~~2~~ 3, wherein the at least one implicit write command includes a command having a format capable of specifying the first region of memory as a non-contiguous region of multiple disconnected sub regions, the memory device access controller having the capability to direct writing to each of the multiple disconnected sub regions in turn.

10. (Original) The memory module buffer of claim 9, the memory device access controller having the capability to respond to a command format specifying a start address, write length, skip length, and number of sub regions, by repetitively writing data to a range of addresses equal to the write length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub

regions has been written.

11. (Currently Amended) The memory module buffer of claim ~~2~~ 3, wherein the write data generator comprises an error correction code generator capable of generating an error correction code as part of an implicit write data word.

12. (Currently Amended) The memory module buffer of claim ~~2~~ 3, the memory device channel port having a data width, the buffer further comprising a data mask generator to mask a portion of the data width during writes responsive to an implicit command type when an implicit command specifies a partial-width write command.

13. (Currently Amended) The memory module buffer of claim ~~1~~ 3, further comprising a pause function activated by the command decoder when a second command requiring access to the memory device channel port is received during activity related to a first command of an implicit command type, the memory device access controller responding to the pause function by pausing execution of the first command while the second command executes.

14. (Currently Amended) The memory module buffer of claim ~~1~~ 3, further comprising a completion register that the memory module buffer sets to indicate the status of a pending command with an implicit command type, wherein the value stored in the completion register is accessible from the host-side memory channel port.

15. (Currently Amended) The memory module buffer of claim ~~1~~ 3, the memory device access controller having the capability to respond to a command format specifying a start address, read length, skip length, and number of sub regions, by repetitively reading data from a range of addresses equal to the read length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub regions has been read.

Claims 16-23 (Cancelled)

24. (Cancelled) A buffered memory module comprising:

a plurality of memory devices; and

a buffer connected to the memory devices and having

a host-side memory channel port,

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type, and

a memory device access controller to respond to a command having an implicit command type by generating and transmitting at least one explicit memory access command to the memory devices.

25. (Currently Amended) The buffered memory module of claim ~~24~~ 26, wherein the at least one implicit command type includes at least one implicit write command with a command format that specifies a first region of memory to be written to and includes less explicit write data than would be needed to fill the region of memory, the buffer

further comprising a write data generator to form implicit write data in accordance with the implicit write command.

26. (Currently Amended) ~~The buffered memory module of claim 24,~~ A buffered memory module comprising:

a plurality of memory devices; and

a buffer connected to the memory devices and having

a host-side memory channel port,

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type, and

a memory device access controller to respond to a command having an implicit command type by generating and transmitting at least one explicit memory access command to the memory devices, the memory device access controller having the capability to respond to a command format specifying a start address, read length, skip length, and number of sub regions, by repetitively reading data from a range of addresses equal to the read length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub regions has been read from the memory devices.

Claims 27-31 (Cancelled)